

## CLAIMS

1. A shift register comprising a level shifter which amplifies an amplitude  
of a clock signal,  
5 wherein the level shifter comprises:  
a capacitor means;  
an inverter of which input portion is connected to a first electrode of the  
capacitor means;  
a means for connecting the input portion and an output portion of the  
10 inverter electrically;  
a first means for inputting a reference potential to a second electrode of the  
capacitor means;  
a second means for inputting the clock signal to the second electrode of the  
capacitor means;  
15 a third means for fixing a potential of an output of the level shifter; and  
a fourth means for fixing a potential of the input portion during a period in  
which the level shifter does not operate, and  
wherein a control signal of the level shifter is generated from an output  
pulse of the shift register.  
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2. The shift register according to claim 1,  
wherein an H-level and an L-level of the clock signal are used as the  
reference potential.
- 25 3. A shift register comprising a level shifter which amplifies an amplitude  
of a clock signal,  
wherein the level shifter comprises:  
a capacitor means;  
a first inverter of which input portion is connected to a first electrode of the  
30 capacitor means;

a second inverter of which input portion is connected to an output portion of the first inverter;

a first switch provided between the input portion and the output portion of the first inverter;

5 a second switch provided between the input portion of the first inverter and a power supply;

a first means for inputting a reference potential to a second electrode of the capacitor means; and

10 a second means for inputting the clock signal to the second electrode of the capacitor means,

wherein the second inverter comprises a third switch for fixing a potential of an output of the level shifter in a period in which an output of the first inverter is unstable; and

15 wherein a control signal of the level shifter is generated from an output pulse of the shift register.

4. A shift register comprising a level shifter which amplifies an amplitude of a clock signal,

20 wherein the level shifter comprises a first inverter and a second inverter connected in series;

a first switch provided between an input portion and an output portion of the first inverter;

a second switch provided between the input portion of the first inverter and a power supply;

25 a first capacitor means and a second capacitor means of which first electrodes are connected to the input portion of the first inverter;

a third switch for inputting an H-level of the clock signal as a reference potential to a second electrode of the first capacitor means;

30 a fourth switch for inputting an L-level of the clock signal as a reference potential to a second electrode of the second capacitor means; and

a means for inputting the clock signal to second electrodes of the first and the second capacitors means,

wherein the second inverter comprises a fifth switch for fixing a potential of an output of the level shifter during a period in which an output of the first inverter is unstable; and

wherein a control signal of the level shifter is generated from an output pulse of the shift register.

5. A shift register comprising a level shifter which amplifies an amplitude of a clock signal,

wherein the level shifter comprises:

a first inverter and a second inverter connected in series;

a first switch provided between an input portion and an output portion of the first inverter;

a second switch provided between the input portion of the first inverter and a power supply;

a first capacitor means and a second capacitor means of which first electrodes are connected to the input portion of the first inverter;

a third inverter of which output portion is connected to a second electrode of the first capacitor means;

a third switch provided between an input portion and an output portion of the third inverter;

a fourth switch provided between the input portion of the third inverter and a power supply;

a third capacitor means of which first electrode is connected to the input portion of the third inverter;

a fifth switch for inputting an H-level of the clock signal to a second electrode of the third capacitor means;

a fourth inverter of which output portion is connected to a second electrode of the second capacitor means;

a sixth switch provided between an input portion and an output portion of the fourth inverter;

a seventh switch provided between the input portion of the fourth inverter and a power supply;

5 a fourth capacitor means of which first electrode is connected to the input portion of the fourth inverter;

a eighth switch for inputting an L-level of the clock signal to a second electrode of the fourth capacitor means; and

a means for inputting the clock signal to second electrodes of the third  
10 capacitor means and a fourth capacitor means,

wherein the second inverter comprises a ninth switch for fixing a potential of an output of the level shifter during a period in which an output of the first inverter is unstable; and

wherein a control signal of the level shifter is generated from an output  
15 pulse of the shift register.

6. The shift register according to any one of claims 1 to 5,

wherein a number of stage of the level shifter and a number of stage of flip-flop which configure the shift register in the ratio of 1 : N (N is two or more).  
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7. A driving method of a shift register comprising a level shifter which amplifies an amplitude of a clock signal,

wherein the level shifter comprises:

a capacitor means;

25 an inverter of which input portion is connected to a first electrode of the capacitor means;

a switch provided between the input portion and an output portion of the inverter;

a first means for inputting a reference potential to a second electrode of the  
30 capacitor means;

a second means for inputting a clock to the second electrode of the capacitor means;

a third means for fixing a potential of an output of the level shifter; and

5 a fourth means for fixing a potential of an input portion of the inverter, comprising

a step of turning ON the switch to set the input portion and the output portion of the inverter to a threshold potential of the inverter in a reset period, thereby setting a first electrode of the capacitor means at the threshold potential and setting the second electrode of the capacitor means to a reference potential by the  
10 first means;

a step of inputting the clock signal to the second electrode of the capacitor means by the second means in a clock receiving period, and outputting the signal according to the clock signal which is inputted an H-level or an L-level by the third means in dependence on a potential change from the reference potential;

15 a step of fixing a potential of an output of the level shifter by the third means during a period in which an output of the inverter is unstable;

a step of fixing a potential of an input portion of the inverter by the fourth means during a period in which the level shifter does not operate; and

a step of generating a control signal of the level shifter from an output pulse  
20 of the shift register.

8. The driving method of the shift register according to claim 7,

wherein an H-level and an L-level of the clock signal are used as the reference potential.

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